Low-Noise InGaAs HEMT Using the New Off-Set Recess Gate Process

Osamu Ishikawa, Katsunori Nishii, Toshinobu Matsuno, Chinatsu Azuma
Yoshito Ikeda , Syutaro Nanbu and Kaoru Inoue

Semiconductor Research Center
Matsushita Electric Industrial Co., Ltd.
3-15, Yagumonakamachi, Moriguchi, Osaka, 570 Japan

ABSTRACT

Low noise InGaAs HEMT (high electron mobility transistor) with noise figure of 0.68 dB at 12 GHz has been developed using the new off-set recess gate process.

The pseudomorphic n-AlGaAs / InGaAs HEMT structure was grown on the semi-insulating GaAs substrate by MBE. The new off-set recess gate process make it possible to decrease the source and gate resistance. The breakdown voltage between gate and drain became higher than 6V. Gm of 510mS / mm at minimum noise bias point has been obtained in a 0.2μm gate InGaAs HEMT.

The minimum noise figure and associated gain of the device are 0.68dB and 10.4dB at Vds=2V, Ids=16mA and f=12GHz, respectively. Three stage amplifier using the new HEMT at the head has showed the minimum noise figure of 1.2dB and the maximum gain of 31dB.

INTRODUCTION

HEMT is widely used as the low noise device in the satellite communication system now. However, demands for super low noise HEMT has been increasing, because it can reduce the size of antenna, can save the time loss of adjusting the system and realize the high performance satellite communication system.

Noise figure of the n-AlGaAs / GaAs HEMT has been saturated near 1.0 dB level. The new hetero structure and process technology are needed to break through that level and to meet the needs of the low noise device.

The key points in the low-noise devices are to achieve 1) high electron velocity, 2)low source resistance, 3)low leakage-current between gate and drain, 4)low gate resistance.[1] n-AlGaAs / InGaAs hetero structure has attracted much attention because of its excellent microwave characteristics. n-AlGaAs / InGaAs hetero structure features the high electron velocity, high transconductance and large current driving capability, compared to the conventional n-AlGaAs / GaAs hetero structure. [2-7] Off-set gate structure is suitable for low noise device owing to its small source resistance. The newly developed off-set recess gate process make it possible to decrease the source and gate resistance, and to increase the breakdown voltage between gate and drain.

This paper describes how we have realized the super low noise HEMT.

DEVICE STRUCTURE & FABRICATION

Figure 1 is the photograph of the HEMT chip used in this work. The total gate width and the channel length are 160 μm and 0.2 μm, respectively. The cross sectional view of the low noise InGaAs pseudomorphic HEMT is shown in Fig.2. This pseudomorphic structure was grown by MBE on a semi-insulating GaAs substrate by the following sequence. Following 5000Å undoped GaAs buffer layer, 150Å InGaAs quantum well, 20Å undoped AlGaAs spacer layer, 250Å n-AlGaAs layer and 1000Å n+-GaAs cap layer are successively grown. The AlAs mole fraction in AlGaAs layer is 0.2 and the doping level of Si is 1.8×10^{18} cm^{-3}. The In mole fraction in InGaAs layer is 0.2.

Our new off-set recess gate process features the good controllability of the gate formation. The gate is off-set near the source to reduce the source resistance. The gate is self-aligned to the recess region and there is no need to align the gate mask to the recess region. The T-shaped gate is hold by the thick SiN walls used in the recess etching process. So, it is very easy to form the low resistance gate. The flow chart of this new off-set recess gate process is shown in Fig. 3. The process is constructed from 5 steps as explained below.

(step A) SiO_2 deposition

SiO_2 layer (The thickness and width of this layer are 500Å and 0.8 μm.) is deposited between the source and drain ohmic electrodes. This SiO_2 layer acts as the buffer to reduce the damage of the dry etching of the SiN layer(step B).

(step B) formation of the the gate window

After deposition of the SiN layer (The thickness is 3000Å.), the gate window of 0.2um is opened at the source side of the deposited SiO_2 layer. The gate window is formed using the dry etching process.

(step C) wet etching of the SiO_2 layer

SiO_2 layer is etched from the gate window. The breakdown voltage is controlled by this step. If SiO_2 layer is etched-off, very high breakdown voltage is achieved.

(step D) recess etching

n+-layer of the substrate is recess-etched from the gate window. The n+-layer of the drain side is widely etched, compare to the source side. So, the source resistance is kept in very low level and breakdown voltage between the gate and the drain becomes high. The breakdown voltage can be controlled by the width of the SiO_2 layer or the etching time of it.

CH2725-0/89/0000-0979$01.00 © 1989 IEEE

(step E) formation of the gate electrode

The total thickness of the T-shaped gate electrode (Au/Pt/Ti) formed by evaporation and electro-plating is about 1.2 μm. The gate electrode is formed using the same window as the recess etching, so our process has a good controllability to form the low-resistance gate.

The SEM photograph of the device after recess etching (see Fig.3 D)) is shown in Fig.4. It is clear that the gate window is opened near the source side of the recess region.

As a result, the source resistance has become lower than 2 ohm and the breakdown voltage between gate and drain higher than 6 V, and Rg (gate resistance) has become 3 ohm, nearly half of the conventional gate.

DC CHARACTERISTICS

DC characteristics of our typical HEMT (Lg=0.2μm and W=160μm) have been measured using the hermetic sealed package. I-V and Gm-Vgs characteristic of the InGaAs HEMT are shown in Fig.5 and Fig.6, respectively. Our HEMTs are enhanced mode type transistor as shown in Fig.5. From Fig.6, Gm of 82 mS (510mS / mm) has been obtained at Vds=2V and Ids=16mA. The device showed the minimum noise figure at that bias point.

BVgdo (breakdown voltage between gate and drain) is 2 times larger than BVgso (breakdown voltage between gate and source) and BVgdo of 6 V has been obtained at the reverse current I_R= 10μA (see Fig.7). It is the effect of the off-set recess gate process.

RF CHARACTERISTICS

The frequency dependence of h_{21} is shown in Fig.8. h_{21} data are transformed from the [S] parameter data. Cut-off frequency f_T of 40 GHz at the optimum bias point for minimum noise figure was estimated from Fig.8 . The minimum noise figure of 0.68dB and associated gain of 10.4 dB at 12 GHz has been obtained at Vds=2V and Ids=16mA, shown in Fig.9.

Three-stage amplifier using the new HEMT at the first stage has been successfully designed and evaluated. The second and the third transistor of the three-stage amplifier are GaAs MESFETs, the noise figure of them is about 1.6 dB at 12 GHz. In Ku band (11.7GHz ~ 12.2 GHz), the amplifier showed the minimum noise figure of 1.2 dB , the return loss of -12 dB and associated gain of 31 dB. (Fig.10) These high performance has been achieved by adopting the n-AlGaAs / InGaAs pseudomorphic HEMT structure and newly developed process technology.

CONCLUSION

Low noise InGaAs HEMT with noise figure of 0.68 dB at 12 GHz has been developed.

The device is realized by using n-AlGaAs / InGaAs HEMT structure and also newly developed off-set recess gate process. Three stage amplifier using the new HEMT has showed the minimum noise figure of 1.2dB and the maximum gain of 31dB in Ku band.

This low noise InGaAs HEMT has the potential to realize the high performance satellite communication system by its superior characteristics.

ACKNOWLEDGMENT

The authors would like to thank Dr. H. Mizuno , Dr. S. Horiuchi and Dr. T. Kajiwara for their encouragement throughout this work.

REFERENCES

[1] H. Fukui, IEEE Trans. on Circuit Theory, vol.CT-13, No.2, pp.137-142, June 1966.

[2] K. Inoue et al., IEDM Tech.Dig., 422 (1987)

[3] K. Nishii et al., Extended Abstract of the 20th Conference on Solid State Device and Material, Tokyo, 543 (1988)

[4] W.t.Masselink et al.,IEDM Tech. Dig.,755 (1985)

[5] T.Henderson et al., IEDM Tech. Dig., 464 (1986)

[6] A. Okamoto et al., GaAs and Related Compounds, 569 (1987)

[7] T. Henderson et al., IEEE Elec. Dev. Lett., EDL-7, 288 (1986)

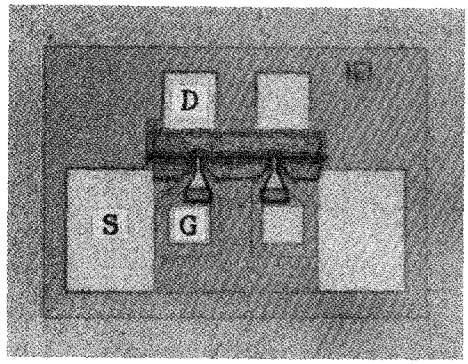

Fig. 1 Photograph of the HEMT chip (Lg=0.2μm, W=160μm)

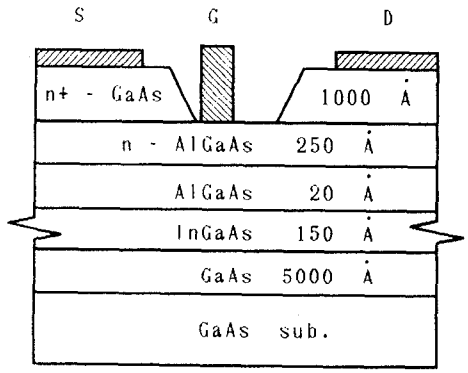

Fig. 2 InGaAs HEMT structure

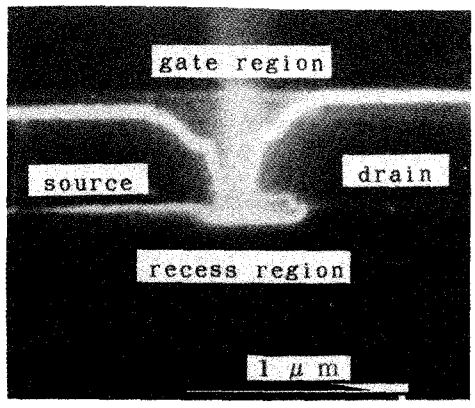

Fig. 4 SEM photograph of the recess region

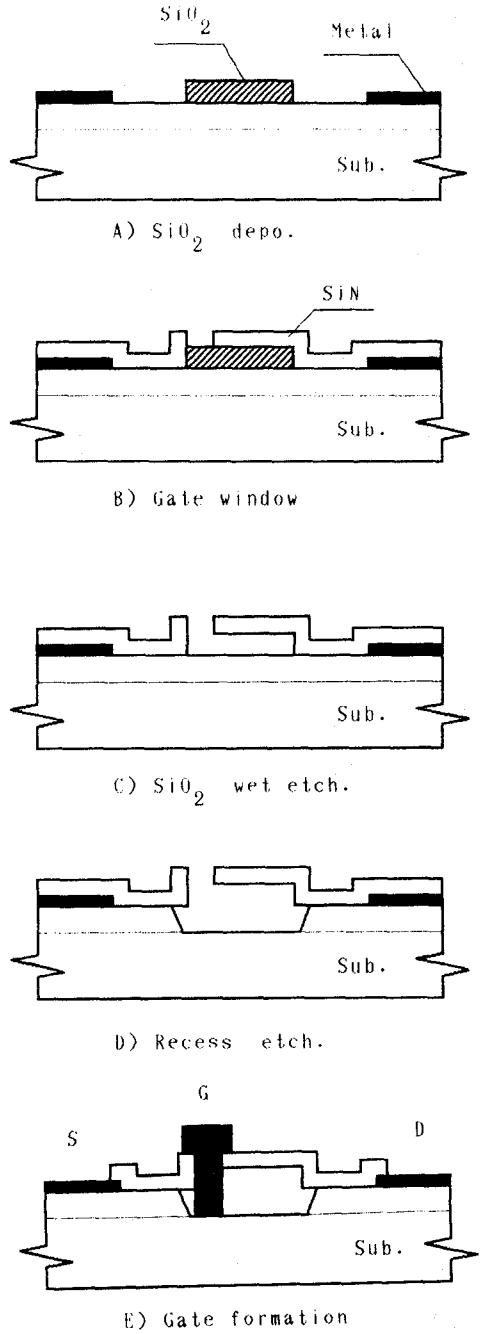

Fig. 3 Flow of the off-set recess gate process

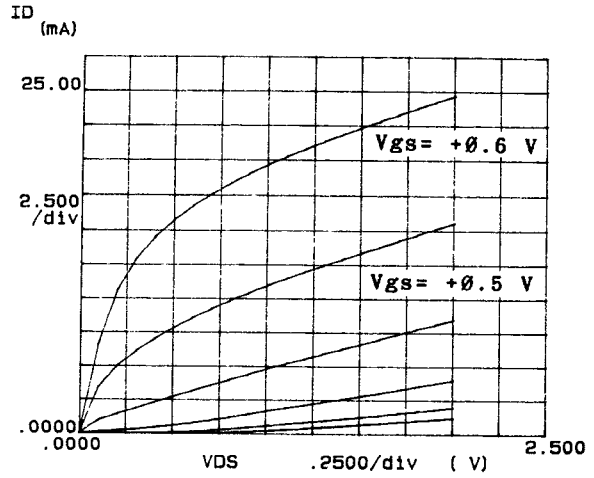

Fig. 5 I-V characteristics of the HEMT (Lg=0.2μm, Wg=160μm)

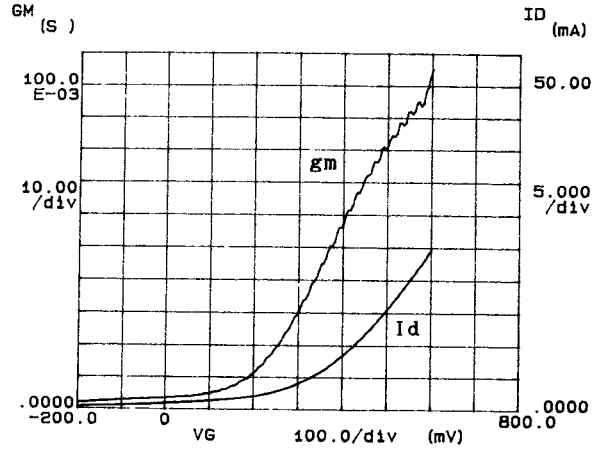

Fig. 6 Gm-Vgs characteristics Gm of 82 mS has been obtained at Vds=2V and Ids=16mA.

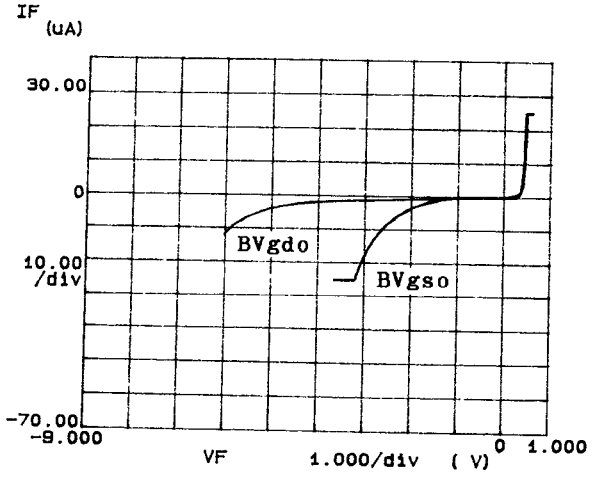

Fig. 7 BVgdo and BVgso

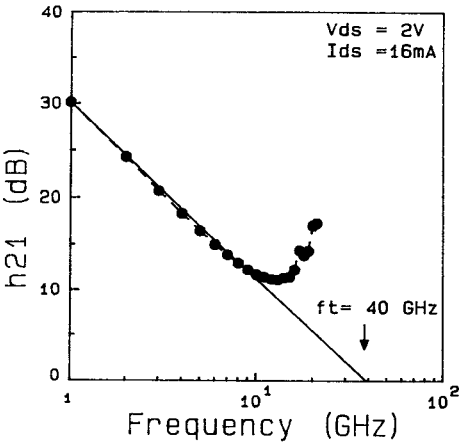

Fig. 8 f_T of the HEMT

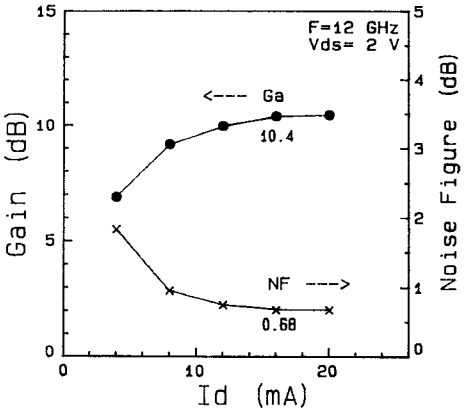

Fig. 9 NF and Ga characteristics The minimum noise figure of 0.68 dB has been obtained at Vds=2V and Ids=16mA.

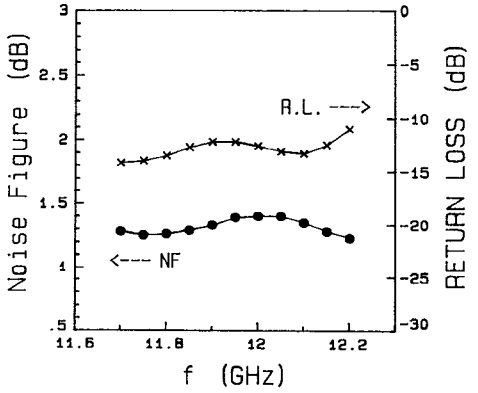

Fig. 10 Noise figure and input return loss of the 3-stage amplifier